IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS

Applicant(s)	Kucharski	**APPEAL BRIEF**
Serial No.	10/056,270	
Filing Date	1/24/2002	
Confirmation No.	8559	
Examiner Name	Tuan T. Dinh	
Group Art Unit	2841	
Attorney Docket No.	100.323US01	
Title: ELECTRICAL NOISE PROTECTION		

1. Introduction

On December 19, 2006, Appellant filed a notice of appeal from the final rejection of claims 1-6, 11-13, 16-17, and 22-24 set forth in the Office Action mailed September 20, 2006. This Appeal Brief is accompanied by a fee in the amount of $500.00 as required under 37 C.F.R. §41.20(b)(2).

2. Real Party in Interest

The real party in interest in the above-captioned application is the assignee, ADC DSL Systems, Inc.

3. Related Appeals and Interferences

Appellant filed one previous appeal in the present patent application. In that previous appeal, on June 3, 2004, Appellant filed a notice of appeal from the final rejection of claims 1-26 set forth in the Final Office Action mailed March 10, 2004 and filed an Appeal Brief in connection with that Appeal on September 7, 2004. The Examiner, in response to Appeal Brief, mailed a new non-final Office Action on December 3, 2004 in which claims 1-6, 11-13, 16, 17, and 22-24 were rejected and claims 7 and 18 were objected to.

There are no other appeals or interferences known to Appellants which will have a bearing on the Board's decision in the present appeal.

4. Status of the Claims

Claims 1-6, 8-17, 19-26 are pending in the application.

Claims 1-6, 11-13, 16-17, and 22-24 were elected for examination and are the subject of this appeal.

Claims 8-10, 14, 15, 19-21, 25, and 26 have been withdrawn from consideration.

In the Final Office Action mailed September 10, 2004, claims 1 and 11-13 were finally rejected under 35 U.S.C. §102(b) and claims 2-6, 16-17 and 22-24 were finally rejected under 35 U.S.C. §103(a).

5. Status of Amendments

No amendment has been filed subsequent to the Final Office Action mailed September 20, 2006.

6. Summary of Claimed Subject Matter

Pursuant to 37 C.F.R. §41.37(c)(1)(v), Appellant provides the following concise explanation of the subject matter defined in each independent claim with reference to the specification by page and line number and to the drawings by reference number. Appellant submits that the citations to the specification and drawings are not intended to be exhaustive and that other support for the various claims may also be found throughout the specification and drawings.

Embodiments of the present invention reduce noise that is transmitted by a power loop of a switch-mode power supply to other circuitry within the switch-mode power supply, such as a sensitive control circuit for controlling the switch-mode power supply. This involves locating the power loop and the other circuitry on opposite sides of a circuit board and respectively connecting the power loop and the other circuitry to electrically interconnected ground planes lying in different planes of the circuit board. This reduces the interference transmitted from the power loop to the other circuitry compared to when the other circuitry and the power loop are located on the same side of the circuit board and/or are connected to the same ground plane.

One embodiment of a switch-mode power supply 100 is shown in Figure 1 of the present application and is described at paragraph [0015], page 3, through paragraph [0017], page 4.

Switch-mode power supply 100 includes a circuit board 101, shown in cross-section in Figure 1. A power loop 102 is disposed on a side (or layer) 110 of circuit board 101. A control circuit 103 is disposed on a side (or layer) 112 of circuit board 101 opposite to side 110. In the embodiment shown in Figure 1, power loop 102 includes a capacitor 120, an inductor 122, and a switch 124. Disposing power loop 102 and control circuit 103 on opposite sides of circuit board 101 physically separates power loop 102 from control circuit 103. This reduces interference transmitted from power loop 102 to control circuit 103 compared to when power loop 102 and control circuit 103 are located on the same side of a circuit board.

Power loop 102 is connected to a ground plane 104 disposed on a layer 130 that is disposed between sides 110 and 112 of circuit board 101. Control circuit 103 is connected to a ground plane 105 on a layer 132 that is disposed between sides 110 and 112 of circuit board 101 so that ground planes 104 and 105 lie in different planes of circuit board 101 and are physically separated from each other. This reduces the interference transmitted to control circuit 103 compared to when control circuit 103 is connected to the same ground plane as power loop 102. In the embodiment shown in Figure 1, a conductive trace 106 disposed within circuit board 101 interconnects ground planes 104 and 105 and a conductive trace 107 connects ground planes 104 and 105, for example, to chassis ground. Control circuit 103 operates at current levels substantially lower than power loop 102.

7. Grounds of Rejection to be Reviewed on Appeal

The first issue presented in this Appeal is whether the Examiner erred in rejecting claims 1-6, and 11-13 under 35 USC § 103(a) as being unpatentable over Akiba et al. (U.S. Patent No. 6,353,540) in view of Theus (U.S. Patent No. 4,904,968).

The second issue presented in this Appeal is whether the Examiner erred in rejecting claims 16-17, and 22-24 under 35 USC § 103(a) as being unpatentable over Akiba et al. (U.S. Patent No. 6,353,540) in view of Theus (U.S. Patent No. 4,904,968).

8. Arguments

A. The Applicable Law

35 U.S.C.§ 103 provides in relevant part:

Conditions for patentability; non-obvious subject matter.

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

To establish a case of *prima facie* obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art and not based in the applicant's disclosure. *In re vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir 1991). MPEP § 2143 - § 2143.03.

The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. MPEP Section 2143.01 *citing In re Mills,* 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990) (Claims were directed to an apparatus for producing an aerated cementitious composition by drawing air into the cementitious composition by driving the output pump at a capacity greater than the feed rate. The prior art reference taught that the feed means can be run at a variable speed, however the court found that this does not require that the output pump be run at the claimed speed so that air is drawn into the mixing chamber and is entrained in the ingredients during operation. Although a prior art device "may be capable of being modified to run the way the apparatus is claimed, there must be a suggestion or motivation in the reference to do so." 916 F.2d at 682, 16 USPQ2d at 1432.).

B. Arguments Relating to Rejection under 35 U.S.C. §103 (a)

The Examiner asserted that Akiba discloses "a first circuit (26, column 18, lines 50-51) disposed on a first side (a top side) . . . a second circuit (28, column 18 line 61) disposed on a second side (a bottom side)." With respect to the language in claim 1 reciting "wherein the first and second ground planes respectively lie in different planes of the circuit board and are electrically interconnected by a conductive trace disposed within the circuit board", the Examiner took the position that ground planes 15 and 21 of Akiba are electrically connected through a resistor Rc as shown in FIG. 34. See, Final Office Action, paragraph 2.

In the Final Office Action, the Examiner stated that Akiba fails to disclose the second circuit operating at current levels substantially lower than the first circuit. However, the Examiner went on to assert that "it would have been obvious to one of skill in the art at the time the invention was made to use the circuit board having the second circuit operating at current levels substantially lower than the first circuit as taught by Theus employed in the device of Akiba et al. in order to provide a radiation [sic] of the unnecessary electromagnetic wave due to the voltage variation between a power source and ground." Final Office Action, paragraph 2.

Appellant submits that the resistor Rc shown in FIG. 34 of Akiba does not comprise "a conductive trace disposed within the circuit board" as set forth in claim 1. Nowhere does Akiba teach or suggest that the resistor Rc of FIG. 34 is a trace. Moreover, Akiba is silent as to having the resistor Rc "disposed within the circuit board" as recited in claim 1 of the present application. It is respectfully submitted that Akiba neither teaches nor suggest this. See, e.g., Akiba, column 18, lines 43-48 ("The matching termination resistor Rc 25 (25-1, 25-2) is connected to the end of the parallel plate line (two lines for the rectangular shape) formed by the ground layer G115 and the ground layer G321 to absorb the potential fluctuation (resonance) of the power layer V116 and the power layer V220.") (emphasis added). Appellant made this argument in a response filed on June 21, 2006, and the Examiner failed to address this argument in the Final Office Action.

Furthermore, Appellant submits that one of ordinary skill in the art would not be motivated to make the proposed combination for the reason the Examiner set forth in the Final Office Action. The motivation to combine the Examiner set forth in the Final Office Action is "to provide a radiation [sic] of the unnecessary electromagnetic wave due to the voltage variation between a power source and ground." Appellant assumes that the Examiner meant to say "to

provide a reduction of the unnecessary electromagnetic wave …"

The Examiner has provided no explanation as how the proposed combination would provide any reduction in unnecessary electromagnetic waves above and beyond simply Akiba by itself (that is, Akiba without the proposed modification). Indeed, Theus clearly indicates that I/O devices operating at current levels substantially higher than the current levels at which logic devices operate is a problematic feature (according to Theus it leads to signal distortion and crosstalk). The proposed combination would add this problematic feature of Theus (I/O devices operating at current levels substantially higher than the logic devices) to Akiba for the stated reason of reducing unnecessary electromagnetic waves. It is respectfully submitted that one of ordinary skill in the art, desiring to reduce unnecessary electromagnetic waves, would simply use Akiba without the proposed modification since the proposed combination, according to Thues, would only add a new source of signal distortion and crosstalk without otherwise reducing unnecessary electromagnetic waves (the Examiner provided no explanation as to how the cross-talk reduction features of Theus (i) would be operable in the proposed combination or (ii) would result in a reduction of unnecessary electromagnetic waves). It is respectfully submitted that the proposed combination is simply the result of applying of impermissible hindsight.

Appellant made this argument in a response filed on June 21, 2006. In the Final Office Action, the Examiner incorrectly characterized Appellant's argument. The Examiner characterized Appellant's argument as arguing that the combination of Akiba and Theus do not teach "the second circuit operates at current levels substantially lower than the first circuit" and went to explain how such features are taught. Final Office Action, paragraph 5. This is not responsive to Appellant's argument since Appellant's argument was directed to the motivation to combine the references.

Claims 2-6 and 11-13 depend from claim 1 and, thus, are allowable for at least the reasons stated above with respect to claim 1.

Accordingly, for the reasons set forth above, the Examiner erred in rejecting claims 1-6, and 11-13 under 35 USC § 103(a) as being unpatentable over Akiba et al. (U.S. Patent No. 6,353,540) in view of Theus (U.S. Patent No. 4,904,968).

It is respectfully submitted that the arguments set forth above with respect to claim 1 apply to claim 16-17 and 22-24 as well.

Accordingly, for the reasons set forth above, the Examiner erred in rejecting claims 16-17, and 22-24 under 35 USC § 103(a) as being unpatentable over Akiba et al. (U.S. Patent No. 6,353,540) in view of Theus (U.S. Patent No. 4,904,968).

Respectfully submitted,

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CLAIMS APPENDIX

1. An electronic device comprising:

a circuit board;

a first circuit disposed on a first side of the circuit board, the first circuit connected to a first ground plane of the circuit board;

a second circuit disposed on a second side of the circuit board, wherein the second side is opposite the first side, the second circuit connected to a second ground plane of the circuit board; and

wherein the first and second ground planes respectively lie in different planes of the circuit board and are electrically interconnected by a conductive trace disposed within the circuit board; and

wherein the second circuit operates at current levels substantially lower than the first circuit.

2. The electronic device of claim 1, wherein the first circuit is a switch-mode power supply.

3. The electronic device of claim 2, wherein the switch-mode power supply is a forward-type switch mode power supply.

4. The electronic device of claim 2, wherein the switch-mode power supply is a flyback-type switch mode power supply.

5. The electronic device of claim 1, wherein the second circuit controls the first circuit.

6. The electronic device of claim 1, wherein the first circuit is adapted to power the second circuit.

11. The electronic device of claim 1, wherein the circuit board comprises two or more layers disposed between the first and second sides.

12. The electronic device of claim 11, wherein the first ground plane is disposed on one of the two or more layers and the second ground plane is disposed on another of the two or more layers.

13. The electronic device of claim 1, wherein the circuit board comprises one or more layers disposed between the first and second sides.

16. A switch-mode power supply comprising:

a circuit board;

a power loop disposed on a first side of the circuit board, the power loop connected to a first ground plane of the circuit board;

a control circuit disposed on a second side of the circuit board, the second side opposite the first side, the control circuit connected to a second ground plane of the circuit board, wherein the control circuit is adapted to control the power loop; and

wherein the first and second ground planes respectively lie in different planes of the circuit board and are electrically interconnected by a conductive trace disposed within the circuit board; and

wherein the control circuit operates at current levels substantially lower than the power loop.

17. The switch-mode power supply of claim 16, wherein the power loop is adapted to power the control circuit.

22. The switch-mode power supply of claim 16, wherein the circuit board comprises two or more layers disposed between the first and second sides.

23. The switch-mode power supply of claim 22, wherein the first ground plane is disposed on one of the two or more layers and the second ground plane is disposed on another of the two or more layers.

24. The switch-mode power supply of claim 16, wherein the circuit board comprises one or more layers disposed between the first and second sides.

EVIDENCE APPENDIX

There is nothing to present in the Evidence Appendix.

RELATED PROCEEDINGS APPENDIX

There is nothing to present in the Related Proceedings Appendix.